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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/749,674	12/27/2000	Min-Cheng Kao	JCLA6439	8688
23900	7590	02/09/2005	EXAMINER	
J C PATENTS, INC. 4 VENTURE, SUITE 250 IRVINE, CA 92618			GERSTL, SHANE F	
			ART UNIT	PAPER NUMBER
			2183	

DATE MAILED: 02/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	<b>Application No.</b>	<b>Applicant(s)</b>	
	09/749,674	KAO ET AL.	
	<b>Examiner</b>	<b>Art Unit</b>	
	Shane F Gerstl	2183	

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
  - If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
  - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
  - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 11 August 2004.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-5 and 8-10 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-5 and 8-10 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some    \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                        | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)    | Paper No(s)/Mail Date. _____  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____   | 6) <input type="checkbox"/> Other: _____                                    |

**DETAILED ACTION**

1. Claims 1-5 and 8-10 have been examined.

***Papers Received***

2. Receipt is acknowledged of amendment and change of address papers submitted, where the papers have been placed of record in the file.

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1, 5, and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hammond (5,638,525) in view of Takayama (6,085,306).

5. In regard to claim 1,

- a. Hammond discloses a data processing apparatus for executing multiple instruction sets comprising:

- i. a memory, for storing a plurality of instruction words of the instruction sets (figure 5, memory);
- ii. a processor core, for executing a primary instruction word of the instruction words (figure 5, element 104);

iii. a plurality of data registers, for storing data of the instruction words;  
[Column 4, lines 10-15 show registers that hold data manipulated by the computer and thus used by the instructions.]

iv. a processor status register for storing a status of the processor core, wherein the processor status register contains an instruction set selector (ISS) for indicating a current instruction set of the instruction sets;  
[Column 14, line 63 – column 15, line 6 shows a signal from the decoder that indicates the instruction set so that the demultiplexer selects the correct path. Thus this signal is an instruction set selector. Column 15, lines 41-52, show that this signal (instruction set selector) is changed based on two jump instructions, or switch instructions. It can be seen throughout Hammond that such instructions are the only way to change this signal. Thus, the ISS must be stored so that the demultiplexer can select the appropriate path for the instructions following such a switch instruction. Since the signal shows the current instruction set it is a processor status and the means for which it is stored in can be called a processor status register. Therefore, the instruction set selector, for indicating a current instruction set, is stored in a process status register.]

v. a predecoder (figure 5, elements 540 and 541) for translating at least one of the instruction sets to the primary instruction word and outputting therewith; [Column 14, lines 18-20, show that the translator, translates one set of instructions into another set of instructions. Lines 21-

29 then go on to show that the new translated instruction set is decoded and executed by the processor and is thus the primary instruction word. The demultiplexer is shown to choose the correct path for the instruction set based on whether it already is the primary instruction word or not.]

vi. An lcache, for storing the primary instruction word (figure 5, element 542). [Since the predecoder outputs the primary instruction word, the lcache stores the primary instruction word.]

vii. a decoder (figure 5, element 543), for decoding the primary instruction word, wherein the processor core is used for executing the word decoded by the decoder; [As shown above, the lcache stores the primary instruction word and since the decoder receives its data from the lcache, it decodes this primary instruction word.]

viii. a bus, being an interface between the predecoder and the memory (figure 5, path from memory to element 540).

b. Hammond does not explicitly disclose a program counter for addressing a next instruction word stored in the memory or program counter control responsive to the instruction set selector to modify the value of the program counter to fit the length of the instruction word, whose length is different from that of the primary instruction word;

c. Takayama has taught in figure 7 the use of program counter control that increments or modifies the program counter. This is further shown in column 11, lines 16-34. This section states that the program counter stores an address of the next instruction that is fetched (using the instruction fetch unit of figure 4 to access memory) and executed. This section also explicitly shows that the reason the program counter is incremented by a value of "4" is because that length of the instruction in bytes.

d. Takayama has shown in column 11, lines 46-53 that the PC unit (program counter and control of figure 7) allows for parallel execution of branch control and the operations unit, which one of ordinary skill in the art would recognize to be a performance benefit since less overall time is spent on execution if portions are done in parallel. This performance benefit would have motivated one of ordinary skill in the art to modify the design of Hammond to include the program counter and control taught by Takayama to address the next instruction for execution. With this program counter and control unit placed in the disclosure of Hammond, Hammond in view of Takayama would have addressed the next instruction in memory by modifying the program counter by a value dependent on the length of the instruction. Since Hammond has disclosed the use of 16 and 32-bit instruction sets in the brief summary, the program counter control would update the program counter by the either 2 or 4 for 16 and 32-bit instructions respectively. This would have been signaled by the instruction set selector (and thus responsive to it), which has been shown to be the indication of the

instruction set and thus its length. If an instruction is not a branch, an incrementation of the PC based on the instruction size is made. Hammond has disclosed the use of multiple instruction sets with different sizes. The combination of Hammond and Takayama must result in program counter control able to choose between the branch and one of multiple increment values depending on the instruction set in use, which as given in Hammond is indicated by an ISS.

It would have been obvious to one of ordinary skill in the art at the time of invention to modify the design of Hammond to implement the program counter and program counter control disclosed by Takayama so that improved system performance would be realized.

6. In regard to claim 5, Hammond in view of Takayama discloses the apparatus of claim 1, as described above, wherein the predecoder contains at least one sub-decoder, for translating at least one of the instruction sets to the primary instruction word. [Since as shown above the translator portion of the predecoder translates an instruction set into the primary instruction word, this translator is in fact a sub-decoder.]

7. In regard to claim 8, Hammond in view of Takayama discloses the apparatus of claim 1, wherein the instruction set selector includes at least one bit. [The instruction set selector is shown by Hammond to be one signal or a second signal (column 15, lines 2-6), or one set of bits or a second set of bits. Thus the instruction set selector must include at least one bit.]

8. Claims 2-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hammond in view of Takayama further in view of Jaggar (5,568,646) and further in view of Hennessy.

9. In regard to claim 2,

a. Hammond in view of Takayama discloses the apparatus of claim 1, as described above;

b. Hammond in view of Takayama does not disclose wherein there are two sets of bits in each of the data registers, at least one bit is viewed as an instruction set selection bit (IS) and the other bits stored in each data register are viewed as a target address (TA).

c. Jaggar has shown in figure 1 and column 3, lines 37-52, a plurality of data registers for that include an instruction set flag (instruction set selection bit). This flag, depending on which register it is located in, indicates the instruction set used by the processor for decoding currently and for past instructions. Hennessy has shown on pages 151-152 the description and illustration of register addressing for branch instructions. This means that a branch instruction branches to an address stored in a register. If one combines these two concepts, the result is a set of registers that indicate an instruction set and hold an address for branching.

d. Jaggar has shown in column 3, lines 44-50, that the instruction set flag can be used for quick exception handling since previous flags are saved. By branching to an address stored in a register, the range of addresses accessible



becomes larger as can be seen by figure 3.17 in Hennessy. The ability to recover quickly from exceptions and to have a greater range of addresses for branching would have motivated one of ordinary skill in the art to modify the invention of Hammond in view of Takayama to include the instruction selection bits in each data register as taught by Jaggar and to branch to addresses stored in the registers as taught by Hennessy.

It would have been obvious to one of ordinary skill in the art to modify the design of Hammond in view of Takayama to include the instruction set selection bits given by Jaggar and the register addressing mode for branching taught by Hennessy so that quick exception handling was achieved while being able to access a wide range of instruction memory through branching.

10. In regard to claim 3, Hammond in view of Takayama further in view of Jaggar and further in view of Hennessy discloses the apparatus of claim 2, as described above, wherein the target address is a starting address of an instruction set. [Hammond shows in column 5, lines 2-8 that the jump address, or branch address, is the beginning of a set of instructions. Figure 2 shows instructions 211, to be of the new instruction set.]

11. In regard to claim 4, Hammond in view of Takayama further in view of Jaggar and further in view of Hennessy discloses the apparatus of claim 2, as described above, wherein the ISS is set by a specified branch instruction according to the IS in the data registers. [The instruction set selector is set on a jump (branch) instruction as shown above. The instruction set will then be in accord with the IS in the current data register, which stores the instruction set of the current instruction as shown above.]

12. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hammond in view of Takayama.

13. In regard to claim 10,

a. Hammond in view of Takayama has disclosed the apparatus of claim 1, wherein the predecoder contains a plurality of sub-decoders, and switching between the sub-decoders is controlled by the ISS. [Figure 5 shows that the demultiplexer of the predecoder switches between using the translation sub-decoder for translation of instructions or not depending on the instruction set given by the controlling ISS from the decoder. This is further shown in column 15, lines 7-18. ]

b. Hammond in view of Takayama has not disclosed that the predecoder contains a plurality of sub-decoders.

c. While a plurality of translators or sub-decoders is not explicitly taught, the switching (based on the ISS) between using directly executable instructions of one instruction for processing and translation of instructions in a second instruction set into instructions in the first instruction set for processing is taught. The inclusion of a plurality of translators or sub-decoders to perform the same function as a single translator, that is selecting an instruction set for translation into the first instruction set, provides no new or unexpected result over the prior art. Therefore, one of ordinary skill in the art would have found it obvious to duplicate the translator or sub-decoder, creating a plurality of translators or sub-decoders for translating instructions from one instruction set into another primary

instruction set (see MPEP 2144.04 (VI): In re Harza, 274 F.2d 669, 671, 124 USPQ 378, 380 (CCPA 1960)).

14. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hammond in view of Takayama and further in view of Jaggar.

15. In regard to claim 9,

a. Hammond in view of Takayama discloses the apparatus of claim 1, as described above;

b. Hammond in view of Takayama does not disclose that the instruction set selector can be set according to one or more instruction set bits of the data registers.

c. Jaggar has shown in figure 1 and column 3, lines 37-52, a plurality of data registers for that include an instruction set flag (instruction set selection bit). This flag, depending on which register it is located in, indicates the instruction set used by the processor for the current and past instructions. Therefore, when Jaggar sets the instruction set selector as shown above on a specified jump (branch) instruction, the instruction set selector is being set in accordance with the instruction set selection bit of the data registers.

d. Jaggar has shown in column 3, lines 44-50, that the instruction set flag can be used for quick exception handling since previous flags are saved. The ability to recover quickly from exceptions would have motivated one of ordinary skill in the art to modify the invention of Hammond in view of Takayama to include the instruction selection bits in each data register as taught by Jaggar.

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It would have been obvious to one of ordinary skill in the art to modify the design of Hammond in view of Takayama to include the instruction set selection bits given by Jaggar so that quick exception handling was achieved.

***Response to Arguments***

16. Applicant's arguments filed 8/11/04 have been fully considered but they are not persuasive.

17. Applicant has argued with respect to claim 1 that Hammond and Takayama does not disclose an "instruction set selector (ISS) for indicating a current instruction set of the instruction sets; ... a program counter control, responsive to the instruction set selector to modify the value of the program counter..." Specifically, it is asserted that Takayama changes the program counter according to encountering a branch or not instead of which instruction set is used and Hammond selects a correct path for decoding instructions but does not teach to modify values of the program counter according to ISS.

18. Hammond has shown in Column 14, line 63 – column 15, line 6 shows a signal from the decoder that indicates the instruction set so that the demultiplexer selects the correct path. Thus this signal is an instruction set selector. As Applicant notes, Hammond does not explicitly disclose a program counter for addressing a next instruction word stored in the memory or program counter control responsive to the instruction set selector to modify the value of the program counter to fit the length of the instruction word, whose length is different from that of the primary instruction word. Takayama has taught in figure 7 the use of program counter control that increments or modifies the program counter. This is further shown in column 11, lines 16-34. This section states that the program counter stores an address of the next instruction that is fetched (using the instruction fetch unit of figure 4 to access memory) and executed. This section also explicitly shows that the reason the program counter is incremented by a value of “4” is because that length of the instruction in bytes. Takayama has shown in column 11, lines 46-53 that the PC unit (program counter and control of figure 7) allows for parallel execution of branch control and the operations unit, which one of ordinary skill in the art would recognize to be a performance benefit since less overall time is spent on execution if portions are done in parallel. This performance benefit would have motivated one of ordinary skill in the art to modify the design of Hammond to include the program counter and control taught by Takayama to address the next instruction for execution. With this program counter and control unit placed in the disclosure of Hammond, Hammond in view of Takayama would have addressed the next instruction in memory by modifying the program counter by a value dependent on

the length of the instruction. Since Hammond has disclosed the use of 16 and 32-bit instruction sets in the brief summary, the program counter control would update the program counter by either 2 or 4 for 16 and 32-bit instructions respectively. This would have been signaled by the instruction set selector (and thus responsive to it), which has been shown to be the only indication given by Hammond of the instruction set and thus the length associated with it.

19. Applicant is correct that the program counter is chosen based on a branch, but, this is not the only consideration. If not a branch, an incrementation of the PC based on the instruction size is made. Hammond has disclosed the use of multiple instruction sets with different sizes. The combination of Hammond and Takayama must result in program counter control able to choose between the branch and one of multiple increment values depending on the instruction set in use, which as given in Hammond is indicated by an ISS.

### ***Conclusion***

20. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

21. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shane F Gerstl whose telephone number is (571) 272-4166. The examiner can normally be reached on M-F 6:45-4:15 (First Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

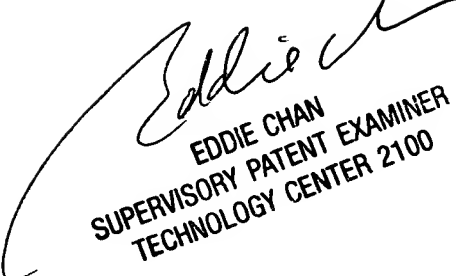
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